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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/607,912	06/30/2000	Douglas E. Duschatko	M-8320 US	1177
33031	7590	02/25/2004	EXAMINER	
CAMPBELL STEPHENSON ASCOLESE, LLP 4807 SPICEWOOD SPRINGS RD. BLDG. 4, SUITE 201 AUSTIN, TX 78759			PHAN, MAN U	
			ART UNIT	PAPER NUMBER
			2665	11

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	09/607,912	Applicant(s)	Duschatko et al.
Examiner	Man Phan	Art Unit	2665

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on Dec 15, 2003

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-16 is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) 13-16 is/are allowed.

6) Claim(s) 1 and 4-10 is/are rejected.

7) Claim(s) 2, 3, 11, and 12 is/are objected to..

8) Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on Mar 30, 2000 is/are a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner. If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some* c) None of:

1. Certified copies of the priority documents have been received.

2. Certified copies of the priority documents have been received in Application No. _____.

3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) The translation of the foreign language provisional application has been received.

15) Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) Notice of References Cited (PTO-892)

4) Interview Summary (PTO-413) Paper No(s). _____

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

5) Notice of Informal Patent Application (PTO-152)

3) Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____

6) Other: _____

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Response to Amendment and argument

1. This communication is in response to applicant's 12/15/2003 Amendment in the application of Duschatko et al. for a "Path AIS insertion for concatenated payloads across multiple processors" filed 06/30/2000. This application claims benefit from Provisional Application 60/211,559 dated 06/15/2000. The proposed amendments have been entered and made of record. Applicant's amendment and arguments to the pending claims have been considered but are not persuasive, and will be examined as discussed below. Claims 1-16 are pending in the application.
2. The corrected or substitute drawings were received on 12/15/2003. These drawings are approved. Applicant is advised to submit new formal drawings including changes required by the proposed drawing correction filed on 12/15/2003, which has been approved by the examiner.
3. Applicant's amendment and argument to the rejected claims are insufficient to distinguish the claimed invention from the cited prior arts or overcome the rejection of said claims under 35 U.S.C.103 as discussed below. Applicants' argument with respect to the amended claims have been fully considered, but they are not persuasive for at least the following reasons:
4. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on

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obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

5. On pages 16-17, applicant asserts that there is no motivation to combine the references i.e., Baydar et al., and Derbenwick et al., as proposed in the Office Action. In response, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Baydar et al. (US#5,717,693) and Derbenwick et al. (US#6,262,975) applied herein for the teaching of a method and apparatus for improve the pointer processing in SONET transmission frame utilizing Alarm Insertion Signal (AIS) detection.

6. Applicant's argument with respect to the rejected claims 1, 4 and 7 (Page 13, first and second paragraphs) that the cited references do not teach or suggest "the demultiplexer nor the demultiplexing". However, Baydar et al. teaches in Fig. 1b block diagram illustrated a receive

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section of a SONET pointer processing integrated circuit including the multiplexing/demultiplexing in signal processing (*specified as blocks 4g and 4nq in Fig. 1b*). As illustrated in Fig. 1b, at the receive local interface (4), at which SONET data from a SONET line are received and demultiplexed into individual STS-1 data streams (demultiplexer (4g) for demultiplexing the multiplexed frame data signal (4f) into a plurality of frame data signals). These data are passed to a pointer processing unit (4c) for reading pointer data from a frame data signal, and interpreting the pointer value extracted (Baydar: Col. 1, lines 62 to Col. 2, lines 35). The use of demultiplexer for demultiplexing multiplexed frame data received is well known in the SONET transmission system, and demultiplexing is a typically part of the receive circuit for receiving an incoming SONET signal, and for detecting an alarm condition therefrom. Consequently, in accordance with the Baydar's invention, because the pointer provides immediate access to the start of an synchronous payload envelope (SPE) frame, any other position or timeslot within the SPE is also immediately accessible. This capability should be compared to the procedures required to demultiplex a pre-SONET, asynchronous DS3. Thus, the pointer is able to accommodate differences not only in the phases of the STS/STM SPE/VC and the transport overhead, but in the frame rates as well (Baydar: Col. 2, lines 13-24). Therefore, examiner maintains that the references cited and applied in the last office actions for the rejection of the claims 1-12 are maintained in this office action.

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Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103© and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 1, 4-6 and 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baydar et al. (US#5,717,693) in view of Derbenwick et al. (US#6,262,975).

With respect to claims 1, 4-6 and 7-10, both Baydar et al. (US#5,717,693) and Derbenwick et al. (US#6,262,975) disclose a novel method and system for quickly generating

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and transmitting SONET AIS signals according to the essential features of the claims. Baydar discloses a SONET payload pointer processing and its transport overhead architecture. Figs. 1a&b block diagrams illustrated a SONET pointer processing integrated circuit, comprising a demultiplexer (4nq) having an input for coupling to the payload and having plurality of outputs (4np); a multiplexer (4g) having a plurality of inputs; a plurality of pointer processors (4b, c), each having an input coupled to the respective input of the multiplexer, wherein each of the pointer processors comprises a bidirectional terminal coupled to a common node (Col. 3; lines 29 plus and Col. 6, lines 20 plus). Baydar further teaches in Fig. 20 illustrated the VT (Virtual Tributary structures - sub-STS mapping uses in SONET standard) elastic store counters, in which each of the 28 counters 463a is incremented in its VT time slot by a hard-wired pulse on a line 463c from a demultiplexer 463d which is responsive to the VT# (TRADR) signal on the line 2i and to an enable (EN) signal on a line 463e. VT alarm registers block 350 stores two alarm signals for each independent VT pointer. VT path AIS on the line 346 and VTLOP on a line 470 are stored into flip-flops synchronously in the corresponding VT time slots. Once these flip-flops are set, they are not reset until they are read. They are read out on a line by the microprocessor interface as 4-bit groups carrying information for two VTs. If one of the VT path AIS or VTLOP bits is active, a VT error is generated and stored in a separate register set whose outputs are provided on a line 474 and multiplexed with the tributary addresses in a VT Data Multiplexer of a VT pointer generation block 476 shown in Fig. 4D and Fig. 31b in detail (Col. 19, lines 60 plus).

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However, Baydar does not expressly disclose the circuitry for causing a logic level to be asserted at the common node in response to an error signal at the processor input, and wherein the alarm means is included as a component of a concatenated payload. In the same field of endeavor, Derbenwick et al. discloses a method for auditing cross-connection provisioned to carry a concatenated signal in a optical transport system, in which the incoming signals are monitored and the outputting of a signal is blocked if the pattern of output channels assigned to that signal is not correct. This is particularly useful for ensuring that a concatenated signal in a SONET transport system is transported correctly over contiguous channels. Specifically, the Derbenwick teach the process for detecting different trigger states associated with the processing of a particular incoming signal, and responsive to detecting the presence of one of the trigger states and responsive to a determination that the incoming signal is of a particular type, then the process determines if a pattern of outputs paths specified for the incoming signal meet a predetermined criterion and inserts an alarm signal in the specified output paths in place of the incoming signal if the predetermined criterion is not met. Advantageously, then, the Derbenwick's invention allows a communications system to output a concatenated signal only when contiguous channels have been assigned to that signal (See Fig. 5; Col. 1, lines 65 plus and Col. 4, lines 48 plus).

One skilled in the art would have recognized the need for effectively and efficiently providing a method and system for quickly generating and transmitting SONET AIS signals when pointer processor detects a fault in a concatenated payload signal, and would have applied

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Derbenwick's novel use of the auditing process that provisioned to carry a concatenated signal into Baydar's overhead pointer processing for a synchronous optical network (SONET).

Therefore, It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to apply Derbenwick's method of auditing cross-connections related to concatenated signals in SONET into Bardar's SONET payload pointer processing and architecture with the motivation being to provide a method and system for the generation of a path alarm insertion signal (AIS) at the output of concatenated pointer processors.

Allowable Subject Matter

4. Claims 2-3 and 11-12 are objected to as being dependent upon the rejected base claims, but would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims.

10. Claims 13-16 are allowable. These are new amended claims which include the allowable subject matter set forth in the office action mailed on 10/28/2003.

6. The following is an examiner's statement of reasons for the indication of allowable subject matter: The closest prior art of record fails to disclose or suggest the steps wherein the bidirectional terminal of each of the plurality of processors is coupled to the common node and

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the common node is coupled through a resistance to a voltage V+, so that in the absence of an alarm signal at all the processor inputs, the voltages at the bidirectional terminals of the processors approaches V+, and wherein as a result of an error signal at the input of any processor, the voltages at the bidirectional terminals of all the processors approach a reference voltage, as specifically recited in claims 2, 3; wherein the alarm means comprises an error detector, a wired-OR logic element coupled between the error detector and the bidirectional terminal; and a combinational logic element having inputs respectively coupled to the output of the processor, as specifically recited in claim 11.

11. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The Parruck (US#5,265,096) is cited to show the SONET alarm indication signal transmission method and apparatus.

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The Fukunaga et al. (US#6,118,795) is cited to show the reception pointer processing apparatus in SDH transmission system.

The Uematsu et al. (US#5,751,720) is cited to show the pointer processor and pointer processing scheme for SDH/SONET transmission system.

The Lino (US#5,335,223) is cited to show the pointer processing circuit in SONET system.

The Denton et al. (US#6,041,043) is cited to show the SONET path/ATM physical layer transmi/receive processor.

The Rossi et al. (US#6,683,890) is cited to show the method and circuit for improving the pointer processing in SDH transmission frames.

The Hiramoto (US#5,471,476) is cited to show the synchronous payload pointer processing system in digital data transmission network.

13. **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

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CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Mphan

02/20/2004

Manu Phan
MAN PHAN
PATENT EXAMINER